What is claimed is:

1. A method comprising:

receiving an indication of bits of incoming data from a first serial bus;

buffering the bits to accommodate a difference between a first rate of the incoming data and a second rate of outgoing data;

during the buffering, detecting whether at least some of the bits indicate a synchronization field.

2. The method of claim 1, further comprising:

after the buffering, communicating the bits to a second serial bus to form the outgoing data.

3. The method of claim 2, wherein the communicating comprises:

selectively enabling a transmitter based on the detection.

4. The method of claim 3, further comprising:

determining whether the indication of the bits indicates valid bit logic levels; and

further basing enablement of the transmitter on the determination.

5. The method of claim 1, wherein the receiving comprises:

receiving an indication of at least one analog signal from the first serial bus; and

converting the indication of said at least one analog signal into indications of at least some of the bits.

6. The method of claim 1, wherein the buffering comprises:

passing the bits through a delay line.

7. The method of claim 1, wherein the detecting comprises:

comparing at least some of the bits to an indication of a predetermined bit pattern.

8. A repeater comprising:

a data recovery circuit to receive an indication of bits of incoming data from a first serial bus and buffer the bits to accommodate a difference between a first rate of the incoming data and a second rate of outgoing data; and

a synchronization detection circuit coupled to the data recovery circuit to detect, while the data recovery circuit buffering the bits, whether at least some of the bits indicate a synchronization field.

9. The repeater of claim 8, further comprising:

a transmitter to receive an indication of the bits from the data recovery circuit and use the indication from the data recovery circuit to communicate the bits to a second serial bus to form the outgoing data.

10. The repeater of claim 9, wherein the synchronization circuit selectively enables the transmitter based on the detection by the synchronization detection circuit.

11. The repeater of claim 10, further comprising:

a squelch detection circuit to indicate whether valid bit logic levels are present on the first serial bus,

wherein the synchronization circuit selectively enables the transmitter further based on the indication from the squelch detection circuit transmitter.

12. The repeater of claim 10, further comprising:

an analog-to-digital conversion circuit to receive an analog signal from the first serial bus and convert the analog signal into an indication of at least some of the bits.

13. The repeater of claim 10, wherein the data recovery circuit comprises:

a delay line to delay the bits by multiple cycles of a clock signal.

14. The repeater of claim 10, wherein the synchronization detection circuit comprises:

a comparator to compare at least some of the bits to an indication of a predetermined bit pattern to perform the detection.

15. A system comprising:

a first serial bus;

a second serial bus; and

a repeater coupled to the first and second serial busses to receive an indication of bits of incoming data from the first serial bus, and concurrently buffer the bits to accommodate a difference between a first rate of the incoming data and a second rate of outgoing data and detect whether at least some of the bits indicate a synchronization field.

16. The system of claim 15, wherein the repeater comprises:

a receiver to receive an indication of bits of the incoming data from the first serial bus; and

a transmitter to communicate the bits to a second serial bus to form the outgoing data.

17. The system of claim 16, further comprising:

a synchronization circuit to detect the synchronization field and selectively enable the transmitter in response to the detection.

18. The synchronization circuit of claim 16, wherein the synchronization detection circuit comprises:

a comparator to compare at least some of the bits to an indication of a predetermined bit pattern to perform the detection.

19. The system of claim 15, further comprising:

a squelch detection circuit to enable communication to the second serial bus based on whether valid bit logic levels are present on the first serial bus.

20. The system of claim 15, further comprising:

an analog-to-digital conversion circuit to receive an analog signal from the first serial bus and convert the analog signal into an indication of at least some of the bits.